REMARKS

This request for continued examination is being filed in response to the final rejection dated December 12, 2005. Enclosed herewith is a Terminal Disclaimer in order to overcome the rejection of Claims 30-36 under the judicially created doctrine of obviousness-type double patenting over Claims 1-4 of U.S. Patent No. 6 154 191 and Claims 1-4 of U.S. Patent No. 6 424 329.

Claim 32 has been rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification. Specifically speaking, the Examiner states that there is no description in the specification that the constant voltage erases the image displayed on the nematic liquid crystal panel. Applicants respectfully disagree with this rejection. On page 9, lines 9-11, it is stated that an image displayed on a liquid crystal panel in a frame period is erased within the same frame period according to the present invention. This description, in combination with the changes of optical transmittance in Figure 2, provides support for the claimed subject matter that the constant voltage erases the image. Therefore, the Examiner's rejection of Claim 32 under 35 USC 112, first paragraph, is felt to be in error.

Claims 30-33, 35 and 36 have been rejected under 35 USC 102(b) as being anticipated by Yamashita et al. Claim 34 has been rejected under 35 USC 103(a) as being unpatentable over Yamashita et al and further in view of Miyawaki. Applicants respectfully disagree with this ground of rejection.

In paragraph 5 of the Office Action, the Examiner states that Yamashita et al applies a voltage corresponding to image data in response to a pulse G1 and applies a constant voltage (VITO) in response to a second selection pulse G2. However, the constant voltage (VITO) is applied to one of the electrodes (31 of Figure 1), regardless of the state of the gate. Further, it is apparent from Figure 2, that the first

selection pulse G1 and the second selection pulse G2 are connected to different lines. As such, the Examiner is in error regarding these pulses G1 and G2 as being equivalent to the first and second pulses in Claims 30 and 35.

In order to apply an image-independent voltage in Figure 2 of Yamashita et al, it is necessary to open the gate by applying again a pulse to the line of G1 and to simultaneously apply a constant voltage to all sources. Referring to Figure 1 in combination, it is only disclosed to apply the source voltage via the video terminal 1 through switch 4. The switch 4 only affects switching between positive and negative voltages and both of these voltages are image-responsive voltages. Switch 4 does not switch image-responsive voltage and image-independent voltage. As the source voltage, only image-responsive voltages apply. As such, Claims 30-33, 35 and 36 are not only not anticipated by Yamashita et al, these claims are patentably distinguishable thereover.

With respect to the rejection of Claims 32 and 33, although there is a horizontal blanking period in the image signal at the top of Figure 2 of Yamashita, there is no such period in the source voltage. Figure 2 shows a horizontal period and does not show a frame. Although the Examiner contends that Yamashita et al teaches the erasing of the image, or displaying black, at intervals between the application of the image-responsive voltage and a certain period, an application at the same of the next period, perhaps with reference to Figure 2, there is no such teaching in Figure 2 or any other figures. If the Examiner sees "intervals" at the portion between the terminal end of the first serrated signal (labeled ANALOG SIGNAL) and the initial end of the second serrated signal (again labeled ANALOG SIGNAL) in Figure 2 it should be noted that nothing is latched in the source in this period and how a constant voltage for erasing the image or to display black can be applied. Moreover, the Miyawaki reference does not provide these teachings. Therefore, it is respectively submitted that Claim

34 also is patentably distinguishable over the prior art cited by the Examiner.

Favorable consideration of the present application is respectfully solicited.

Respectfully submitted,

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Encl: None

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